Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-33 (Canceled)

Claim 34 (Currently amended): An interconnection apparatus comprising:

a plurality of first ~~substrate~~ substrates;

a plurality of contact structures attached to said first ~~substrate~~ substrates; and

a second substrate comprising:

a plurality of first terminals on a first side thereof,

a plurality of second terminals on a second side thereof, said second side opposite said first side, and

a plurality of interconnections through said second substrate electrically connecting ones of said first terminals with ones of said second terminals;

wherein said first ~~substrate is~~ substrates are attached to said second substrate, and ones of said contact structures are electrically connected to ones of said first terminals,

said plurality of contact structures is for contacting dice of a semiconductor wafer, and

each said first substrate corresponds to one of (i) at least one of said dice or (ii) a portion of one of said dice and a portion of an adjacent die.

Claim 35 (Previously presented): The interconnection apparatus of claim 34, wherein said first terminals are disposed in a first pattern on said first side of said second substrate, and said second terminals are disposed in a second pattern on said second side of said second substrate, and wherein said first pattern is different than said second pattern.

Claim 36 (Previously presented): The interconnection apparatus of claim 35, wherein said first terminals in said first pattern are in a tighter pitch than said second terminals in said second pattern.

Claim 37 (Previously presented): The interconnection apparatus of claim 34 further comprising an electrical interface to a semiconductor tester, wherein ones of said second terminals are electrically connected to said interface.

Claim 38 (Previously presented): The interconnection apparatus of claim 37 further comprising a probe card, wherein said probe card comprises said interface.

Claims 39 and 40 (Canceled)

Claim 41 (Currently amended): The interconnection apparatus of ~~claim 40~~ claim 34, wherein each said first substrate corresponds to one of said dice.

Claim 42 (Currently amended): The interconnection apparatus of ~~claim 40~~ claim 34, wherein each said first substrate corresponds to a plurality of said dice.

Claim 43 (Currently amended): The interconnection apparatus of ~~claim 40~~ claim 34, wherein contact structures are attached to each said first substrate in a pattern that corresponds to a pattern of contacts on one of said dice.

Claim 44 (Currently amended): The interconnection apparatus of ~~claim 40~~ claim 34, wherein contact structures are attached to each said first substrate in a pattern that corresponds to a pattern of contacts on at least two of said dice.

Claim 45 (Currently amended): The interconnection apparatus of ~~claim 40~~ claim 34, wherein contact structures are attached to each said first substrate in a pattern that corresponds to a ~~partial pattern of contacts on~~ portion of one of said dice and a ~~partial pattern of contacts on~~ portion of an adjacent die.

Claim 46 (Previously presented): The interconnection apparatus of claim 34, wherein each of said contact structures comprises a wire.

Claim 47 (Previously presented): The interconnection apparatus of claim 46, wherein each of said contact structures further comprise an overcoat enveloping at least a portion of said wire.

Claim 48 (Currently amended): ~~The interconnection apparatus of claim 47, wherein~~ An interconnection apparatus comprising:

a first substrate;

a plurality of contact structures attached to said first substrate; and

a second substrate comprising:

a plurality of first terminals on a first side thereof,

a plurality of second terminals on a second side thereof, said second side opposite said first side, and

a plurality of interconnections through said second substrate electrically connecting ones of said first terminals with ones of said second terminals;

wherein said first substrate is attached to said second substrate, and ones of said contact structures are electrically connected to ones of said first terminals,

wherein each of said contact structures comprises a wire and an overcoat enveloping at least a portion of said wire, and

said overcoat comprises a material having a greater yield strength than said wire.

Claims 49-62 (Canceled)

Claim 63 (Currently amended): An interconnection apparatus comprising:

a plurality of first ~~substrate~~ substrates, each said first substrate comprising:

a plurality of contact structures attached to a first side of said first substrate,

a plurality of first terminals on a second side of said first substrate, said second side opposite said first side, and

a plurality of interconnections through said first substrate electrically connecting ones of said contact structures with ones of said first terminals; and

a second substrate comprising a plurality of second terminals;

wherein said first ~~substrate is~~ substrates are attached to said second substrate, and ones of said first terminals are electrically connected to ones of said second terminals,

said plurality of contact structures are for contacting dice of a semiconductor wafer, and each said first substrate corresponds to at least one of said dice.

Claims 64 and 65 (Canceled)

Claim 66 (Currently amended): The interconnection apparatus of ~~claim 65~~ claim 63 ~~further comprising a plurality of said first substrates~~, wherein each said first substrate corresponds to one of said dice.

Claim 67 (Currently amended): The interconnection apparatus of ~~claim 65~~ claim 63 ~~further comprising a plurality of said substrates~~, wherein each said first substrate corresponds to a plurality of said dice.

Claim 68 (Previously presented): The interconnection apparatus of claim 63, wherein each of said contact structures comprises a wire.

Claim 69 (Previously presented): The interconnection apparatus of claim 68, wherein each of said contact structures further comprise an overcoat enveloping at least a portion of said wire.

Claim 70 (Currently amended): ~~The interconnection apparatus of claim 69, wherein~~ An interconnection apparatus comprising:

a first substrate comprising:

a plurality of contact structures attached to a first side of said first substrate,

a plurality of first terminals on a second side of said first substrate, said second side opposite said first side, and

a plurality of interconnections through said first substrate electrically connecting ones of said contact structures with ones of said first terminals; and

a second substrate comprising a plurality of second terminals;

wherein said first substrate is attached to said second substrate, and ones of said first terminals are electrically connected to ones of said second terminals,

wherein each of said contact structures comprises a wire and an overcoat enveloping at least a portion of said wire, and

said overcoat comprises a material having a greater yield strength than said wire.

Claims 71-80 (Canceled)

Claim 81 (New): An interconnect structure comprising:

a plurality of first substrates, each said first substrate having a plurality of electrically conductive probes attached thereto; and

a second substrate comprising a plurality of electrical connectors configured to provide an interface for test signals for testing at least one electronic device,

wherein said first substrates are attached to said second substrate such that said probes are disposed in a pattern that corresponds to input and/or output terminals of said at least one electronic device, and

ones of said probes are electrically connected to ones of said electrical connectors.

Claim 82 (New): The interconnect structure of claim 81, wherein said electronic device comprises a semiconductor die.

Claim 83 (New): The interconnect structure of claim 82, wherein said die is one of a plurality of dice of an unsingulated semiconductor wafer.

Claim 84 (New): The interconnect structure of claim 83, wherein the probes attached to each one of said first substrates are configured to correspond to the terminals of one of said dice.

Claim 85 (New): The interconnect structure of claim 83, wherein the probes attached to each one of said first substrates are configured to correspond to the terminals of a plurality of said dice of said wafer.

Claim 86 (New): The interconnect structure of claim 83, wherein the probes attached to each one of said first substrates are configured to correspond to a portion of the terminals of one of said dice and a portion of the terminals of another of said dice.

Claim 87 (New): The interconnect structure of claim 81, wherein each of said probes comprises a spring structure.

Claim 88 (New): The interconnect structure of claim 87, wherein each of said probes is configured to make a pressure based electrical connection with one of said terminals of said at least one electronic device while pressed against said terminal.

Claim 89 (New): The interconnect structure of claim 81, wherein each of said probes are resilient, elongate structures that extend from a surface of the first substrate to which said probe is attached.

Claim 90 (New): The interconnect structure of claim 81, wherein each of said probes comprises a wire and an overcoat enveloping at least a portion of said wire, said overcoat comprising a material having a greater yield strength than said wire.

Claim 91 (New): The interconnect structure of claim 81, wherein said interconnect structure comprises a probe card assembly for probing at least one die of a semiconductor wafer to test said at least one die.